REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for the courtesies extended in the telephonic Examiner Interview of September 12, 2005 and for carefully considering the present application.

Disposition of Claims

Claims 1-7 and 9-13 are pending in the present application. Claims 1, 7, 9, and 13 are independent. The remaining claims depend, directly or indirectly, from claims 1, 7, 9, and 13.

Claim Amendments

Independent claim 1 has been amended to clarify that "at least one of the output from the high comparator and the output from the low comparator is operatively connected to a clock input of a logic device. "[1] No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 2 of the present application.

Independent claim 9 has been amended to clarify that "at least one of the first signal and the second signal is operatively connected to a clock input of a logic device." [1] No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 2 of the present application.

[1] Applicant notes that the Interview Summary of September 21, 2005 recites that the language "wherein at least one of the high comparator output and the low comparator output is connected to a clock input of a *flip-flop circuit*" was agreed to by Applicant and the Examiner in the Examiner Interview of September 12, 2005. However, as subsequently indicated to the Examiner by Applicant, during the actual Examiner Interview, Applicant and the Examiner had agreed to the language "wherein at least one of the output from the high comparator and the output from the low comparator is operatively connected to a clock input of a *logic device.*" Claims 1 and 9 have been amended accordingly.

Drawings

Applicant respectfully requests that the Examiner accept the drawings submitted on March 24, 2004. Applicant submits that these drawings are formal.

Rejection(s) under 35 U.S.C. § 102

Claims 1, 2, 4-6, 9, and 10 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,412,332 issued to Bartonek (hereinafter "Bartonek"). As discussed above, independent claims 1 and 9 have been amended in this reply to clarify the present invention recited. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

The present invention is directed to a method and apparatus for detecting a noise error of a signal. With reference to Figure 2 of the Specification, a noise margin self-diagnostic circuit **50** in accordance with one embodiment of the present invention comprises comparators **58** and **60**, delay buffers **68a**, **68b**, and flip-flops **62a-62d**. In the exemplary embodiment of the present invention shown in Figure 2, the output of high comparator **58** is connected to the clock inputs of flip-flops **62a** and **62c**, while the output of low comparator **60** is connected to the clock inputs of flip-flops **62b** and **62d** (*see, e.g.,* Specification, page 4, line 17 – page 5, line 2). In other words, the outputs of the high comparator **58** and low comparator **60** provide the clock input for flip-flops **62a-62d**.

Transitions from high to low may be measured by flip-flops **62a** and **62b**, delay buffer **68a**, and XOR gate **64a**. Alternatively, transitions from low to high may be measured by flip-flops **62c** and **62d**, delay buffer **68b**, and XOR gate **64b** (*see e.g.,* Specification, page 5, line 18 – page 6, line 8). If no error occurs on a voltage transition (as shown, *e.g.,* in Figure 1A), circuit **50** indicates a normal state at alarm output **70**. However, if there is a noise error (as

shown, *e.g.*, in Figures 1B, 1C, or 1D), the logic of circuit **50** indicates an error at alarm output **70** (*see, e.g.*, page 6, lines 9-16).

Accordingly, amended independent claim 1 requires, in part, that at least one of the output from the high comparator and the output from the low comparator is operatively connected to a clock input of a logic device. Amended independent claim 9 requires that at least one of the first signal and the second signal is operatively connected to a clock input of a logic device.

Bartonek, in contrast to the present invention and as agreed to by the Examiner in the telephonic Examiner Interview of September 12, 2005, does not disclose connecting a compared output signal to a clock input of a logic device. Specifically, Bartonek does not disclose, as required by amended independent claim 1, that at least one of the output from the high comparator and the output from the low comparator is operatively connected to a clock input of a logic device. Further, Bartonek does not disclose, as required by amended independent claim 9, that at least one of the first signal and the second signal is operatively connected to a clock input of a logic device. Further, Bartonek does not show or suggest these limitations. Additionally, Bartonek does not disclose detecting a noise error of a circuit.

Bartonek is directed to a dragger that detects objects dragging beneath a train as the train travels along a track. As Bartonek clearly states, an output signal is generated only when the magnitude of an impact is greater than a predetermined magnitude (*see* Bartonek, abstract). In other words, in contrast to the present invention, Bartonek checks whether a signal becomes greater than a maximum value or less than a minimum value. The purported alarm circuitry of Bartonek merely discloses detecting the presence of a physical fault, such as a short or an open circuit (e.g., due to a break in a sensor cable). To accomplish this, Bartonek discloses detecting when a signal is greater than a maximum sensor voltage or when the signal is less than a

minimum signal voltage (*see* Bartonek, col. 5, line 54, col. 6, line 14). On the other hand, the present invention determines a number of possible signal transitions (noise errors) across a high voltage boundary or a low-voltage boundary. The detection disclosed by Bartonek is clearly different than detecting a noise error as disclosed by the present invention.

Further, as discussed above, Bartonek is completely silent with respect to at least one of the output from the high comparator and the output from the low comparator being operatively connected to a clock input of a logic device. Bartonek clearly does not contemplate using clocked logic devices, as is evidenced by the lack of such devices in both the figures and text of Bartonek.

In view of the above, Bartonek fails to show or suggest the present invention as recited in amended independent claims 1 and 9 of the present application. Thus, amended independent claims 1 and 9 are patentable over Bartonek. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Rejection(s) under 35 U.S.C. § 103

Claims 3, 7, and 11-13 were rejected under 35 U.S.C. § 103 as being obvious over Bartonek in view of U.S. Patent No. 6,275,074 issued to Hastings (hereinafter "Hastings") and U.S. Patent No. 5,923,191 issued to Nemetz *et al.* (hereinafter "Nemetz"). Independent claims 1 and 9 have been amended in this reply to clarify the present invention recited. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

Bartonek, as discussed above, fails to disclose all the limitations of amended independent claims 1 and 9 of the present application. Further, Bartonek fails to disclose all the limitations of independent claims 7 and 13 of the present application. Specifically, Bartonek does not show or suggest high-to-low or low-to-high sub-circuits, where each of these circuits

comprise a plurality of flip-flop circuits that are clocked dependent on one or more compared signals. As discussed above, Bartonek clearly does not show or suggest operatively connecting a comparator output to the clock input of a logic device. Further, as discussed above, Bartonek is not directed to detecting noise errors as required by the present invention.

Like Bartonek, Hastings fails to disclose all the limitations of independent claims claims 1, 7, 9, or 13 of the present application. Further, Hastings does not show or suggest that which Bartonek lacks. This is evidenced by the fact that Hastings is used by the Examiner merely in an attempt to render obvious claim limitations relating to delay buffers and logic gates (*see* Office Action dated July 14, 2005, page 4). Hastings is directed to a system for propagating a digital signal through a slew-rate limited node (*see* Hastings, abstract). Hastings is completely silent with respect to high-to-low or low-to-high sub-circuits, as required by independent claims 7 and 13 of the present application. Further, Hastings is completely silent with respect to detecting noise errors, as required by the claimed invention.

Nemetz, like Bartonek and Hastings discussed above, fails to disclose all the limitations of independent claims 1, 7, 9, or 13 of the present application. Further, Hastings does not show or suggest that which Bartonek and Hastings lack. This is evidenced by the fact that Nemetz is used by the Examiner merely in an attempt to render obvious claim limitations relating to flip-flop circuits (*see* Office Action dated July 14, 2005, page 4). In clear contrast to the present invention, Nemetz is directed to monitoring a system clock signal by comparing pulse widths of logic pulses to a system clock duty cycle (*see* Nemetz, abstract). Nemetz is completely silent with respect to high-to-low or low-to-high sub-circuits, as required by independent claims 7 and 13 of the present application. Further, Nemetz is completely silent with respect to detecting noise errors, as required by the present invention.

Further, Applicant notes that the various combinations of one or more of three references have been used in rejecting the claims of the present application. The purported reconstruction of the claimed invention by reliance on this collection of references ranging from, for example, disclosing a dragger for a train (U.S. Patent No. 6,412,332) to a system and method for monitoring a clock signal of a computer system (U.S. Patent No. 5,923,191) is not appropriate. It is abundantly clear that the Examiner, using the present application as a guide, has selected isolated features of the various relied-upon references to arrive at the limitations of the claimed invention. Use of the present application as a "road map" for selecting and combining prior art disclosures is wholly improper. *See Interconnect Planning Corp. v. Feil*, 774 F.2d 1132 (Fed. Cir. 1985) (stating that "[t]he invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time"); *In re Fritch*, 972 F.2d 1260 (Fed. Cir. 1992) (stating that "it is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious . . . . This court has previously stated that 'one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.'"); *In re Wesslau*, 353 F.2d 238 (C.C.P.A. 1965) (stating that "it is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art").

Further, Applicant notes that there is no motivation to combine the cited references. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. There must be a suggestion or motivation to combine the references *within the prior*

art references themselves. In other words, regardless of whether prior art references can be combined, there must an indication within the prior art references expressing desirability to combine the references. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990) (emphasis added). Further, the present application *cannot be used a guide* in reconstructing elements of prior art references to render the claimed invention obvious. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added).

One skilled in the art would not be motivated by Bartonek, which is directed to a detector to detect objects dragging beneath a train, to incorporate the teachings of Hastings and Nemetz without the present application as a guide. The Examiner assumes that it would have been obvious to one skilled in the art to implement the teachings of Hastings into Bartonek to reduce propagation delays of a current state that is slew-rate limited due to inductances. Further, the Examiner assumes that it would have been obvious to one skilled in the art to implement the teachings of Nemetz into Bartonek to generate one or more error signals for detected pulse width violations by logic high and low comparators. However, Bartonek provides no motivation to reduce propagation delays or to monitor clock signals by comparing pulse width signals and clock signals. This is evidenced by, for example, the fact that Bartonek is *completely silent* with respect to clocking *any* device. Thus, one skilled in the art would not be motivated by Bartonek to incorporate the teachings of Hastings or Nemetz. Further, Bartonek, Hastings, and Nemetz are silent with respect to detecting noise errors as required by the present invention. One skilled in the art would not be motivated by any of the cited prior art, which is completely silent with respect to noise errors, to incorporate the teachings of one another without the present application as a guide. Thus, there is no motivation to combine the cited references.

In view of the above, Bartonek, Hastings, and Nemetz, (i) are not properly combinable under 35 U.S.C. § 103, and (ii) whether taken separately or in any combination, fail

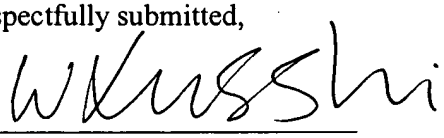
to show or suggest the present invention as recited in independent claims 1, 7, 9, and 13. Thus, independent claims 1, 7, 9, and 13 are patentable over Nemetz. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 06145/003001; P4928).

Dated: October 14, 2005

Respectfully submitted,

By 

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